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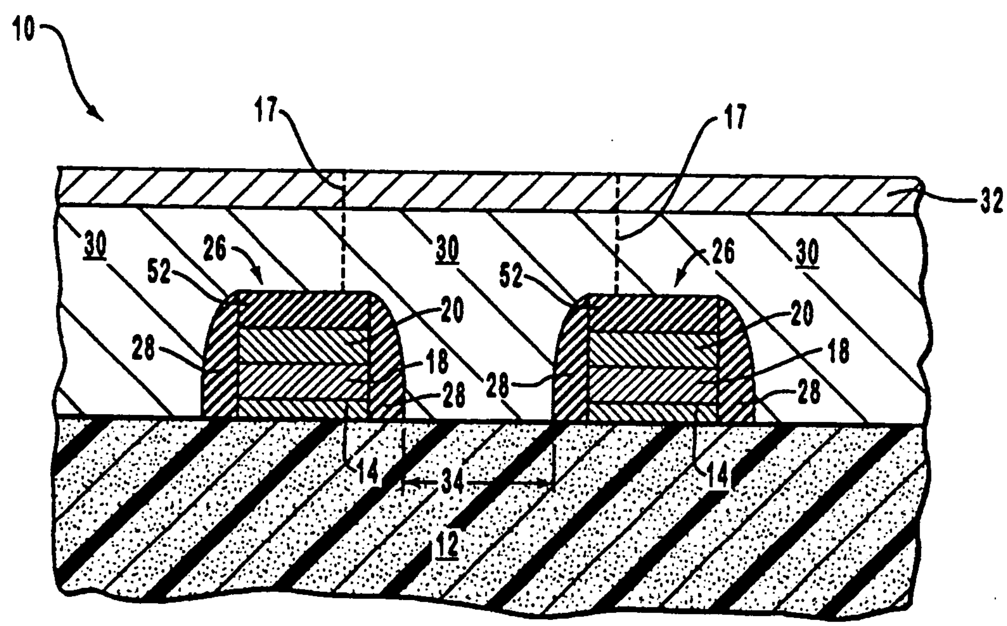



(57) Abstract

The present invention relates to a process for selectively plasma etching a structure upon a semiconductor substrate (12) to form designated topographical structure thereon utilizing an undoped silicon dioxide layer (22) as an etch stop. In one embodiment, a substantially undoped silicon dioxide layer (22) is formed upon a layer of semiconductor material (12). A doped silicon dioxide layer (30) is then formed upon said undoped silicon dioxide layer (16). The doped silicon dioxide layer (30) is etched to create the topographical structure. The etch has a material removal rate that is at least 10 times higher for doped silicon dioxide (30) than for undoped silicon dioxide (16) or the semiconductor material.

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# UNDOPED SILICON DIOXIDE AS ETCH STOP FOR SELECTIVE ETCH OF DOPED SILICON DIOXIDE

## BACKGROUND OF THE INVENTION

### 1. The Field of the Invention

The present invention involves an etching process that utilizes an undoped silicon dioxide layer as an etch stop during a selective etch of a doped silicon dioxide layer that is situated on a semiconductor substrate. More particularly, the present invention relates to a process for selectively utilizing a fluorinated chemistry in a plasma etch system for etching a doped silicon dioxide layer situated upon an undoped silicon dioxide layer that acts as an etch stop.

### 2. The Relevant Technology

Modern integrated circuits are manufactured by an elaborate process in which a large number of electronic semiconductor devices are integrally formed on a semiconductor substrate. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including but not limited to bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term substrate refers to any supporting structure including but not limited to the semiconductive substrates described above.

Conventional semiconductor devices which are formed on a semiconductor substrate include capacitors, resistors, transistors, diodes, and the like. In advance manufacturing of integrated circuits, hundreds of thousands of these semiconductor devices are formed on a single semiconductor substrate. In order to compactly form the semiconductor devices, the semiconductor devices are formed on varying levels of the semiconductor substrate. This requires forming a semiconductor substrate with a topographical design.

The semiconductor industry is attempting to increase the speed at which integrated circuits operate, to increase the density of devices on the integrated circuits, and to reduce the price of the integrated circuits. To accomplish this task, the semiconductor devices used to form the integrated circuits are continually being increased in number and decreased in dimension in a process known as miniaturization.

One component of the integrated circuit that is becoming highly miniaturized is the active region. An active region is a doped area in a semiconductor substrate that is used together with other active regions to form a diode or a transistor. The miniaturization of the active region complicates the formation of the interconnect structure in that, in order to maintain sufficient electrical communication, the interconnect structure must be formed in exact alignment with the active region. Also, the area of the interconnect structure interfacing with the active region must be maximized. Thus, less area is provided as tolerance for misalignment of the interconnect structure.

The increasing demands placed upon manufacturing requirements for the interconnect structure have not been adequately met by the existing conventional technology. For example, it is difficult at greater miniaturization levels to exactly align the contact hole with the active region when patterning and etching the contact hole. As a result, topographical structures near the bottom of the contact hole upon the active region can be penetrated and damaged during etching of the contact hole. The damage reduces the performance of the active region and alters the geometry thereof, causing a loss of function of the semiconductor device being formed and possibly a defect condition in the entire integrated circuit. To remedy these problems, the prior art uses an etch stop to prevent over etching.

In a conventional self-aligned etch process for a contact hole, a silicon nitride layer or cap is usually used on top of a gate stack as an etch stop layer during the self-aligned contact etch process. One of the problems in the prior art with forming a silicon nitride cap was the simultaneous formation of a silicon nitride layer on the back side of the semiconductor wafer. The particular problems depend on the process flow. For instance, where a low pressure chemical vapor deposition is used to deposit silicon nitride, both sides of the semiconductor wafer would receive deposits of silicon nitride. The presence of the silicon nitride on the back side of the semiconductor wafer causes stress which deforms the shape of the semiconductor wafer, and can also potentially cause deformation of the crystal structure as well as cause defects in the circuit. Additionally, silicon nitride deposition is inherently a dirty operation having particulate matter in abundance which tends to reduce yield. When a low pressure chemical vapor deposition process is utilized, the silicon nitride layering on the back side of the semiconductor wafer must be removed later in the process flow.

## SUMMARY OF THE INVENTION

The present invention relates to a process for selectively plasma etching a semiconductor substrate to form a designated topographical structure thereon utilizing an undoped silicon dioxide layer as an etch stop. In one embodiment, a substantially undoped silicon dioxide layer is formed upon a layer of semiconductor material. A doped silicon dioxide layer is then formed upon the undoped silicon dioxide layer. The doped silicon dioxide layer is etched to create a topographical structure. The etch has a material removal rate that is at least 10 times higher for doped silicon dioxide than for the undoped silicon dioxide or the layer of semiconductor material.

One application of the inventive process includes a multilayer structure situated on a semiconductor substrate that comprises layers of a semiconductor material, a thin silicon dioxide layer, a layer of conductor material, and a refractory metal silicide layer. By way of example, the multilayer structure situated on a semiconductor substrate may consist of a gate oxide situated on a silicon substrate, a layer of polysilicon, and a refractory metal silicide layer on the layer of polysilicon. A substantially undoped silicon dioxide layer is then formed over the multilayer structure.

The multilayer structure is then patterned to form the designated topography. Doped silicon dioxide is then formed on the semiconductor substrate as a passivation layer. A photoresist layer is utilized to expose selected portions of the doped silicon dioxide layer that are intended to be etched. One example of a topographical structure created utilizing this process are gate stacks. The doped silicon dioxide is then selectively and anisotropically etched with a carbon fluorine etch recipe so as to self-align contact holes down to the semiconductor substrate between the gate stacks.

Each gate stack has a cap composed of substantially undoped silicon dioxide. A layer of silicon nitride or undoped silicon dioxide is deposited over the gate stacks and the semiconductor substrate therebetween. A spacer etch is performed to create silicon nitride or undoped silicon dioxide spacers on the side of each gate stack. The silicon nitride or undoped silicon dioxide spacers are generally perpendicular to the base silicon layer.

The present invention contemplates a plasma etching process for anisotropic etching a doped silicon dioxide layer situated on an undoped dioxide layer that acts as an etch stop. One application of the present invention is the formation of gate stacks having spacers composed of substantially undoped silicon dioxide. The undoped silicon dioxide spacers act as an etch stop. Novel gate structures are also contemplated that use a

substantially undoped silicon dioxide etch stop layer for a carbon fluorine etch of a doped silicon dioxide layer, where the substantially undoped silicon dioxide etch stop layer resists etching by a carbon fluorine etch.

## BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages and objects of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope, the invention will be described with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is a partial cross-sectional elevation view of one embodiment of a multilayer structure prior to an etch, the multi-layer structure including a base silicon layer and a layer of undoped silicon dioxide, where the multi-layer structure has a layer of photoresist, and wherein a first selected pattern is defined in phantom.

Figure 2 is a partial cross-sectional elevation view of the structure seen in Figure 1, wherein the layer of undoped silicon dioxide has been etched so as to form a recess terminating upon the base silicon layer, a layer of doped silicon dioxide has been deposited thereover, where a layer of photoresist is formed over the layer of doped silicon dioxide, and wherein a second selected pattern is defined in phantom which is intended to represent an etch through the layer of doped silicon dioxide to expose a contact on the base silicon layer that is self-aligned between the layer of undoped silicon dioxide, wherein the self-alignment of the etch is due to the selectivity of the etch to undoped silicon dioxide.

Figure 3 is a partial cross-sectional elevation view of one embodiment of a multilayer structure prior to an etch, the multilayer structure including a base silicon layer and having thereon layers of gate oxide, polysilicon, tungsten silicide, and undoped silicon dioxide, where the multi-layer structure has a layer of photoresist, and wherein a first selected pattern is defined in phantom.

Figure 4 is a partial cross-sectional elevation view of the structure seen in Figure 3, wherein gate stacks are formed upon the base silicon layer, each gate stack having a spacer on a sidewall thereof and a cap on the top thereof, the gate stacks having deposited thereover a layer of doped silicon dioxide, and a layer of photoresist is deposited upon the layer of doped silicon dioxide, wherein a second selected pattern is defined in phantom which is intended to represent a fluorinated chemical etch through the layer of doped silicon dioxide to expose a contact on the base silicon layer that is self-aligned

between the gate stacks, wherein the self-alignment of the etch is due to the selectivity of the etch to the materials of the spacers and the cap of the gate stacks.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The inventive process herein is directed towards selectively utilizing a plasma etch system on doped silicon dioxide ($SiO_2$) layer with a substantially undoped silicon dioxide layer as an etch stop. One application of the inventive process is to form a self-aligned contact. The present invention also discloses an inventive multilayer gate structure.

As illustrated in Figure 1, one embodiment of a multilayer structure 10 is created that comprises a base silicon layer 12. Overlying silicon base layer 12 is a substantially undoped silicon dioxide layer 22. Undoped silicon dioxide layer 22 can be any type of undoped oxide and be formed by a thermal process, by a plasma enhanced deposition process, or by a conventional TEOS precursor deposition that is preferably rich in carbon or hydrogen, or by a precursor of gaseous silane ($SiH_4$) with oxygen. In the latter process, the gaseous silane flow will result in undoped silicon dioxide layer 22.

The next layer in the embodiment of multilayer structure 10 illustrated in Figure 1 comprises a photoresist layer 24 that is processed to expose a first selected pattern 15, shown in phantom, such that silicon dioxide layer 22 will be used to create a topography in multilayer structure 10. Multilayer structure 10 is then anisotropically etched as shown by first selected pattern 15 to selectively remove material from undoped silicon dioxide layer 22 to form undoped silicon dioxide caps 16 as seen in Figure 2.

A doped silicon dioxide layer 30 is deposited over multilayer structure 10 as a passivation layer. Preferably, doped silicon dioxide layer 30 is substantially composed of borophosphosilicate glass (BPSG), borosilicate glass (BSG), or phosphosilicate glass (PSG). Most preferably, doped silicon dioxide layer 30 is substantially composed of silicon dioxide having doping of about 3% or more for boron and about 3% or more for phosphorus. A photoresist layer 32 is applied over doped silicon dioxide layer 30. Photoresist layer 32 is processed to expose a second selected portion 17 of doped silicon dioxide layer 30 that is intended to be etched. Second selected portion 17 is seen in phantom in Figure 2.

The structure seen in Figure 2 is now etched with a fluorinated or fluoro-carbon chemical etchant system to form second selected pattern 17 as illustrated in Figure 2. The preferred manner is an anisotropic plasma etch of doped silicon dioxide layer 30 down to the corresponding etch stop layer of undoped silicon dioxide cap 16. The plasma etch technique employed herein is preferably generated under a vacuum within the confines of a discharging unit and involves any type of a plasma system, including

a high density plasma etcher. A conventional radio frequency reactive ion etcher (RF RIE) plasma system, a magnetically enhanced RIE (MERIE) plasma system, or an inductively coupled plasma system could be used. The preferred embodiment, however, is an RF type RIE or MERIE plasma system. It is preferred the plasma system being used has a plasma density in a range from about $10^9$ /cm$^3$ to about $10^{11}$ /cm$^3$ A high density plasma system can also be used having a plasma density in a range from about $10^{12}$ /cm$^3$ to about $10^{13}$ /cm$^3$

One particular embodiment of a specific structure created utilizing the inventive process is illustrated in Figure 3 wherein a multilayer structure 50 is created that comprises a base silicon layer 12. Overlying silicon base layer 12 is a gate oxide layer 14 that covers silicon base layer 12. Gate oxide layer 14 may be relatively thin in comparison with the other layers of the multilayered structure. The next layer in multilayer structure 50 comprises a polysilicon gate layer 18. Overlying polysilicon gate layer 18 is a refractory metal silicide layer 20. A known benefit of refractory metal silicides is their low resistivity. Refractory metal silicide layer 20 may comprise any refractory metal including but not limited to titanium, tungsten, tantalum, and molybdenum. Preferably, refractory metal silicide layer 20 is substantially composed of tungsten silicide ($WSi_x$).

Overlying refractory metal silicide layer 20 is a substantially undoped silicon dioxide layer 22 which can be formed thermally, by plasma enhanced deposition, by a conventional TEOS precursor deposition that is preferably rich in carbon or hydrogen, or by a precursor of gaseous silane ($SiH_4$) with oxygen. The next layer in multilayer structure 50 is a photoresist layer 24 that is processed to expose a first selected pattern 15 shown in phantom. Multilayer structure 50 is then etched according to first selected pattern 15 to selectively remove material so as to form gate stacks 26 as illustrated in Figure 4. Each gate stack 26 has an undoped silicon dioxide cap 52 thereon which was formed from undoped silicon dioxide layer 22.

A spacer 28 in on the sidewall of each gate stack 26. Spacers 28 are formed by subjecting a layer of silicon nitride deposited over gate stacks 26 to a spacer etch. Silicon nitride spacers 28 are generally perpendicular to silicon base layer 12. Alternatively, spacers 28 can be substantially composed of undoped silicon dioxide. As such, both spacers 28 and undoped silicon dioxide caps 52 can be made from the same materials and both act as an etch stop.

Once gate stacks 26 are formed, a contact 34 is defined therebetween upon silicon base layer 12. At this point in the processing, a doped silicon dioxide layer 30, composed of a material such as PSG, BSG, or BPSG, is deposited over multilayer structure 50. A photoresist layer 32 is then applied over doped silicon dioxide layer 30. Photoresist layer 32 is processed to create a second selected pattern 17 that is illustrated in phantom in Figure 4.

The structure seen in Figure 4 is now etched with a fluorinated or fluoro-carbon chemical etchant system according to second selected pattern 17. The preferred manner of etching of doped silicon dioxide layer 30 down to its corresponding etch stop layer, which is substantially undoped silicon dioxide layer 52, is by a plasma etch. The etch technique employed herein is preferably a plasma etch involving any type of a plasma system including a high density plasma etcher as previously discussed relative to Figure 2.

One factor that effects the etch rate and the etch selectivity of the process is pressure. The total pressure has a preferred range from about 1 millitorr to about 400 millitorr. A more preferred pressure range for a plasma etch is in a pressure range from about 1 millitorr to about 100 millitorr. The most preferred pressure range for a plasma etch is from about 1 millitorr to about 75 millitorr. The pressure may be increased, however, above the most preferred ranges. For example, the RIE etch may be performed at about 100 millitorr. Selectivity can be optimized at a pressure range between about 10 millitorr and about 75 millitorr. Pressure increases may result in a loss in selectivity. The range in selectivity, however, can be adjusted to accommodate different pressures. As such, selectivity and pressure are inversely related.

Temperature is another factor that effects the selectivity of the etching process used. A preferable temperature range during the plasma etch has a range of about 10°C to about 80°C, and more preferably about 20°C to about 40°C. This is the temperature of a bottom electrode adjacent to silicon layer 12 during the etching process. The preferable range of the semiconductor materials is between about 40°C and about 130°C, and more preferably between about 40°C and about 90°C.

Undoped silicon dioxide cap 52 and silicon nitride spacers 28 protect gate stacks 26 from the fluorinated chemical etch. As illustrated in Figure 4, the etch will selectively and anisotropically remove doped silicon dioxide layer 30 above contact 34 as indicated by second selected pattern 17. The etch removes material from doped silicon dioxide layer 30 at a higher material removal rate than that of undoped silicon dioxide

cap 52 and silicon nitride spacers or undoped silicon dioxide spacers 28. Preferably, the etch has a material removal rate for doped silicon dioxide is at least 10 times higher than that of undoped silicon dioxide. As such contact 34 is self-aligned between spacers 28 of gate stacks 26. The self-aligning aspect of contact 34 is due to the selectivity of the etch which assures that even in cases of misalignment of the exposure of second selected pattern 17, the fluorinated chemical etch through doped silicon dioxide layer 30 will properly place contact 34 on silicon base layer 12 and between adjacent silicon nitride spacers 28 that have been formed upon sides of gate stacks 26.

Contact 34 is preferably exposed by an anisotropic plasma etch with a fluorinated chemistry that etches through BSG, PSG, BPSG, or doped silicon dioxide in general. The etch is preferably selective to undoped silicon dioxide, silicon, and silicon nitride. The fluorinated chemical etch utilizes a type of carbon fluorine gas from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $C_2F_8$, $CH_2F_2$, $CHF_3$, $C_2HF_5$, $CH_3F$ and combinations thereof. There are other fluorinated enchants in a substantially gas phase during the etching of the structure. An inert gas is often used in combination with the fluorinated etchant. Argon, nitrogen, and helium are examples of such an inert gas. The preferred gasses, however, are $CF_4$, $CH_2F_2$, $CHF_3$ and Ar. Alternatively $CH_3F$ may be used in place of $CH_2F_2$. In particular, the preferred enchant is a fluorine deficient gas which is defined as a gas where there are not enough fluorine atoms to saturate the bonding for the carbon atoms.

A conductive material is formed upon contact 34 between spacers 28 within second selected pattern 17 as shown in Figure 4. The conductive material will form a contact plug to contact 34. It may be desirable to clad the contact plug with a refractory metal or a refractory metal silicide. As such, second selected pattern 17 would have proximate thereto the refractory metal or silicide thereof prior to formation of the contact plug in contact with contact 34.

The present invention has application to a wide variety of structures. The top layer of the gate stack, composed of undoped silicon dioxide, can be used to create and protect various types of structures during the doped silicon dioxide etching process for structures other than gate stacks.

The present invention allows the gate stack height to be reduced. One advantage of reducing the gate stack height is to reduce the process time which results in greater throughput. The reduced gate height results in a lower etch time and a reduced contact hole aspect ratio, the latter being defined as the ratio of height to width of the contact

hole. By reducing the aspect ratio, or by reducing the height of the gate stack, there will be a decrease in the etch time. Another advantage of a lower gate stack height is that it reduces the overall topography which in turn results in it being easier to planarize and to use photolithographic processes. As such, the present invention increases yield.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed and desired to be secured is:

1. A process for forming a contact opening to a semiconductor material, said process comprising:

(a) forming a substantially undoped silicon dioxide layer over a layer of semiconductor material;

(b) forming a doped silicon dioxide layer over said undoped silicon dioxide layer; and

(c) selectively removing a portion of said doped silicon dioxide layer at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for said layer of semiconductor material to form an opening extending to a contact surface on said layer of semiconductor material.

2. A process as recited in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises:

(a) forming a layer of photoresist over said doped silicon dioxide layer;

(b) patterning said layer of photoresist; and

(c) etching said doped silicon dioxide layer through the pattern of said layer of photoresist.

3. A process as recited in Claim 1, wherein the semiconductor material is monocrystalline silicon.

4. A process as recited in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises a plasma etching process for etching said doped silicon dioxide layer in a plasma etcher.

5. A process as recited in Claim 4, wherein said plasma etching process has a plasma density in a range from about $10^9$ /cm$^3$ to about $10^{13}$ /cm$^3$

6. A process as recited in Claim 4, wherein said plasma etching process is conducted in a pressure range from about 1 millitorr to about 400 millitorr.

7. A process as recited in Claim 4, wherein during said plasma etching process said reactor cathode has a temperature range from about 10°C to about 80°C.

8. A process as recited in Claim 4, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

9. A process as defined in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with an etchant selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $C_2F_8$, $CH_2F_2$, $CHF_3$, $C_2HF_5$, and $CH_3F$.

10. A process as defined in Claim 9, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with an etchant selected from the group consisting of $CH_2F_2$ and $CH_3F$.

11. A process as recited in Claim 1, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with a fluorinated chemical etchant.

12. A process as recited in Claim 1, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG.

13. A process for forming contact to a semiconductor material, said process comprising:

(a) forming a substantially undoped silicon dioxide layer over a layer of monocrystalline silicon;

(b) forming a doped silicon dioxide layer over said undoped silicon dioxide layer, said doped silicon dioxide layer being selected from the group consisting of BPSG, PSG, and BSG;

(c) forming a layer of photoresist over said doped silicon dioxide layer;

(d) patterning said layer of photoresist;

(e) etching said doped silicon dioxide layer through the pattern of said layer of photoresist in a plasma etching process in a plasma etcher, said plasma etching process being conducted:

(a) at a pressure range from about 1 millitorr to about 400 millitorr;

(b) a temperature range of the cathode that is from about 10°C to about 80°C;

(c) in a plasma density in a range from about $10^9$ /cm$^3$ to about $10^{13}$ /cm$^3$

(d) with a fluorinated chemical etchant; and

(f) whereby a contact is exposed on said layer of monocrystalline silicon.

14. A process as recited in Claim 13, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

15. A process as recited in Claim 13, wherein said fluorinated chemical etchant comprises an etchant selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $C_2F_8$, $CH_2F_2$, $CHF_3$, $C_2HF_5$, and $CH_3F$.

16. A process as defined in Claim 15, wherein selectively removing said doped silicon dioxide layer comprises etching of said doped silicon dioxide with an etchant selected from the group of $CH_2F_2$ and $CH_3F$.

17. A process as recited in Claim 13, wherein said plasma etching process is conducted at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for said semiconductor material.

18. A process for forming a contact to a semiconductor substrate comprising:

(a) providing a gate oxide layer over the semiconductor substrate;

(b) providing a pair of gate stacks in spaced relation to one another on the semiconductor substrate, each of said gate stacks having at least one conductive layer formed therein and a substantially undoped silicon dioxide layer extending over said conductive layer;

(c) forming a spacer adjacent to each of said gate stacks;

(d) forming a doped silicon dioxide layer over said pair of gate stacks and over said exposed surface on said semiconductor substrate;

(e) selectively removing a portion of said doped silicon dioxide layer between said pair of gate stacks to expose said surface on said semiconductor substrate, while removing substantially less of said undoped silicon dioxide layer over said pair of gate stacks, wherein said etching removes doped silicon dioxide at a material removal rate that is at least 10 times higher than for each of undoped silicon dioxide, the spacer material the spacer material, and the semiconductor substrate.

19. A process as recited in Claim 18, further comprising:

(a) forming polysilicon layer over said gate oxide layer;

(b) forming a refractory metal silicide layer over said polysilicon layer; and

(c) forming a substantially undoped silicon dioxide layer over said refractory metal silicide layer.

20. A process as recited in Claim 19, further comprising selectively removing portions of said substantially undoped silicon dioxide layer, said refractory metal silicide layer, said polysilicon layer, and said gate oxide layer.

21. A process as recited in Claim 18, wherein said gate stack comprises:

(a) said substantially undoped silicon dioxide layer as the top layer thereof;

(b) a refractory metal silicide layer;

(c) a polysilicon layer; and

(d) a gate oxide layer as the bottom layer thereof.

(e)

22. A process as recited in Claim 18, wherein the spacer material is substantially composed of silicon nitride.

23. A process as recited in Claim 18, wherein the spacer material is composed of substantially undoped silicon dioxide.

24. A process as recited in Claim 18, wherein the semiconductor material is monocrystalline silicon.

25. A process as recited in Claim 18, wherein said plasma etcher is selected from the group consisting of an RF RIE etcher, a MERIE etcher, and a high density plasma etcher.

26. A process as recited in Claim 18, further comprising the step of forming a contact plug composed of a conductive material and situated between said pair of gate stacks and over said surface on said semiconductor substrate.

27. A process as recited in Claim 21, wherein said refractory metal silicide layer is tungsten silicide.

28. A process as recited in Claim 18, wherein said doped silicon dioxide layer is selected from the group consisting of BPSG, PSG, and BSG.

29. A process as recited in Claim 18, wherein selectively removing said doped silicon dioxide layer comprises:

(a) forming a layer of photoresist over said doped silicon dioxide layer;

(b) patterning said layer of photoresist; and

(c) etching said doped silicon dioxide layer through the pattern of said layer of photoresist in a plasma etching process in a plasma etcher, said plasma etching process being conducted:

(a) at a pressure range from about 1 millitorr to about 400 millitorr;

(b) a temperature range of reactor cathode that is from about 10°C to about 80°C;

(c) a temperature range of the semiconductor material is from about 40°C to about 130°C;

(d) in a plasma density in a range from about $10^9$ /cm$^3$ to about $10^{13}$ /cm$^3$ and

(e) with a fluorinated chemical etchant.

30. A process as recited in Claim 29, wherein said fluorinated chemical etchants is selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $C_2F_8$, $CH_2F_2$, $CHF_3$, $C_2HF_5$, and $CH_3F$.

31. A process for forming a contact to a semiconductor material comprising:

(a) depositing a gate oxide layer over a layer of silicon of a semiconductor substrate;

(b) depositing a polysilicon layer over said gate oxide layer;

(c) depositing a refractory metal silicide layer over said polysilicon layer;

(d) depositing a substantially undoped silicon dioxide layer over said refractory metal silicide layer;

(e) selectively removing portions of said substantially undoped silicon dioxide layer, said refractory metal silicide layer, said polysilicon layer, and said gate oxide layer so as to form a pair of gate stacks separated by an exposed portion of said silicon layer, each said gate stack having a lateral side substantially perpendicular to said gate oxide layer and being composed of:

(a) said substantially undoped silicon dioxide layer as the top layer thereof;

(b) said refractory metal silicide layer;

(c) said polysilicon layer; and

(d) said gate oxide layer as the bottom layer thereof;

(f) forming a spacer on the lateral side of each said gate stack from a layer of spacer material;

(g) depositing a doped silicon dioxide layer over said pair of gate stacks and over said exposed portion of said silicon layer, said doped silicon dioxide layer being is selected from the group consisting of BPSG, PSG, and BSG; and

(h) etching said doped silicon dioxide layer with a plasma etching system having a plasma density in a range from about $10^9$ /cm$^3$ to about $10^{13}$ /cm$^3$ in an etcher selected from a group consisting of RF RIE, MERIE plasma etching system, and high density plasma etching system, said plasma etching system having a pressure range from about 1 millitorr to about 400 millitorr, said doped silicon dioxide layer being etched between said pair of gate stacks so as to expose said exposed portion of said silicon layer, said etching having a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide, said spacer material, or silicon, said etching of said doped silicon dioxide being conducted with a fluorinated chemical etchant.

32. A process as recited in Claim 31, wherein the spacer material is substantially composed of one of silicon nitride and substantially undoped silicon dioxide.

33. A process as recited in Claim 31, further comprising forming a contact plug composed of a conductive material and situated between said pair of gate stacks and over the exposed portion of said silicon layer.

34. A process as recited in Claim 34, wherein said fluorinated chemical etchant is selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $C_2F_8$, $CH_2F_2$, $CHF_3$, $C_2HF_5$, and $CH_3F$.

35. A process as recited in Claim 31, wherein during etching of said doped silicon dioxide layer with said plasma etching system, the temperature range of said reactor cathode is from about 10°C to about 80°C.

36. A process as recited in Claim 31, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

37. A process for forming a gate structure comprising:

(a) providing a multilayer structure comprising a layer of silicon dioxide over a layer of silicon;

(b) depositing a layer of substantially undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

(c) forming a first layer of photoresist over said layer of undoped silicon dioxide;

(d) patterning said first photoresist layer to form a first pattern;

(e) etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

(f) depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

(g) etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

(h) removing said first layer of photoresist;

(i) depositing a doped silicon dioxide layer over said multilayer structure;

(j) forming a said second layer of photoresist over said layer of doped silicon dioxide;

(k) patterning said second layer of photoresist to form a second pattern;

(l) etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch through said second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for substantially undoped silicon dioxide, photoresist, or nonconductive material;

(m) removing said second layer of photoresist; and

(n) forming a contact plug composed of a conductive material in contact with said contact surface on said layer of silicon.

38. A process as recited in Claim 37, wherein said nonconductive material is one of silicon nitride and substantially undoped silicon dioxide.

39. A process as recited in Claim 37, wherein said carbon fluorine etch is an anisotropic plasma etch using fluorinated chemical etchants selected from a group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $C_2F_8$, $CH_2F_2$, $CHF_3$, $C_2HF_5$, and $CH_3F$.

40. A process as recited in Claim 37, wherein said multilayer structure further comprises layers of gate oxide, polysilicon, and refractory metal silicide.

41. A process as recited in Claim 37, wherein said doped silicon dioxide layer is selected from a group consisting of BPSG, PSG, and BSG.

42. A process as recited in Claim 37, wherein etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch utilizes a plasma etching system selected from a group consisting of RF RIE, MERIE system, and a high density plasma etch system.

43. A process as recited in Claim 37, wherein etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch is a plasma etching process being conducted:

(a) at a pressure range from about 1 millitorr to about 400 millitorr;

(b) a temperature range of reactor cathode that is from about 10°C to about 80°C;

(c) a temperature range of the semiconductor material is from about 40°C to about 130°C;

(d) in a plasma density in a range from about $10^9$/cm3 to about $10^{13}$/cm3; and

(e) with a fluorinated chemical etchant.

44. A process for forming a gate structure comprising:

(a) providing a multilayer structure situated over a layer of silicon and comprising layers of gate oxide, polysilicon, and refractory metal silicide;

(b) depositing a layer of substantially undoped silicon dioxide over said multilayer structure using a precursor having a gaseous silane, hydrogen, and oxygen flow;

(c) forming a first layer of photoresist over said layer of undoped silicon dioxide;

(d) patterning said first photoresist layer to form a first pattern;

(e) etching said layer of undoped silicon dioxide and said multilayer structure through said first pattern to expose a contact surface on at least a portion of said layer of silicon;

(f) removing said first layer of photoresist;

(g) depositing a layer of a nonconductive material over said layer of undoped silicon dioxide and said contact surface on said layer of silicon;

(h) etching said layer of said nonconductive material to thereby create a spacer over a lateral side of said layer of undoped silicon dioxide and over a lateral side of said multilayer structure, said spacer being generally perpendicular to said layer of silicon;

(i) depositing a doped silicon dioxide layer over said multilayer structure and over said contact surface on said layer of silicon, wherein said doped silicon dioxide layer is selected from a group consisting of BPSG, PSG, and BSG;

(j) forming a said second layer of photoresist over said layer of doped silicon dioxide;

(k) patterning said second layer of photoresist to form a second pattern;

(l) etching said layer of doped silicon dioxide and said multilayer structure with a carbon fluorine etch through said second pattern to expose said contact surface on said layer of silicon, said etching having a material removal rate that is at least 10 times greater for doped silicon dioxide than for substantially undoped silicon dioxide, photoresist, or nonconductive material, wherein said carbon fluorine etch is an anisotropic plasma etch using a fluorinated chemical etchant, wherein said etching of said doped silicon dioxide

utilizes a plasma etching system having a plasma density in a range from about $10^9$ /cm$^3$ to about $10^{13}$ /cm$^3$ at a pressure in a range from about 1 millitorr to about 400 millitorr, the temperature range of said reactor cathode during said plasma etch being about 10°C to about 80°C, and the temperature range of the semiconductor material during said plasma etch being in the range of about 40°C to about 130°C;

(m) removing said second layer of photoresist; and

(n) forming a contact plug composed of a conductive material in contact with said contact surface on said layer of silicon.

45. A process as recited in Claim 44, wherein said fluorinated chemical etchant is selected from a group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $C_2F_8$, $CH_2F_2$, $CHF_3$, $C_2HF_5$, and $CH_3F$.

46. A process as recited in Claim 44, wherein said nonconductive material is one of silicon nitride and substantially undoped silicon dioxide.

47. A gate structure comprising:

(a) a pair of gate stacks situated over a base silicon layer, each said gate stack comprising:

(a) a gate oxide layer on said base silicon layer;

(b) a polysilicon gate layer on said gate oxide layer;

(c) a layer of refractory metal silicide on said polysilicon gate layer;

(d) a substantially undoped silicon dioxide cap on said layer of refractory metal silicide;

(b) a spacer in contact with a lateral side of each said gate stack and with said base silicon layer, said spacer being composed of a nonconductive material, each said lateral side of each said gate stack being substantially perpendicular to said base silicon layer;

(c) a contact plug in contact with said base silicon layer composed of a conductive material, and being situated between said pair of gate stacks; and

(d) a layer of doped silicon dioxide over said spacer, over said substantially undoped silicon dioxide cap, and in contact with said contact plug.

48. A gate structure as recited in Claim 47, wherein said nonconductive material is substantially composed of silicon nitride.

49. The gate structure as recited in Claim 47, wherein said nonconductive material is substantially composed of substantially undoped silicon dioxide, and each said spacer is integral with a respective one of said substantially undoped silicon dioxide cap.

50. A method of forming a self-aligned contact, said method comprising:

(a) providing a pair of gate stacks in spaced apart relation to one another on said semiconductor substrate, each of said gate stacks being covered by a substantially undoped silicon dioxide layer;

(b) forming a spacer adjacent to each of said gate stacks;

(c) forming a doped silicon dioxide layer over said pair of gate stacks and over said semiconductor substrate;

(d) forming a layer of photoresist over said silicon dioxide layer;

(e) patterning said layer of photoresist; and

(f) selectively removing a portion of said doped silicon dioxide layer between said pair of gate stacks to expose a contact surface on said semiconductor substrate through said pattern of said layer of photoresist, while removing substantially less of said undoped silicon dioxide layer over said pair of gate stacks than doped silicon photoresist, , said undoped silicon layer being capable of resisting said selective removal process thereby causing said selective removal process to be self-aligning between said pair of gate stacks.

51. A method as recited in Claim 50, wherein said selective removal of said doped silicon dioxide layer comprises etching said doped silicon dioxide layer in a plasma etching process being conducted:

(a) at a pressure range from about 1 millitorr to about 400 millitorr;

(b) a temperature range of the cathode that is from about 10°C to about 80°C;

(c) in a plasma density in a range from about $10^9$ /cm$^3$ to about $10^{13}$ /cm$^3$ and

(d) with a fluorinated chemical etchants.

52. A method as recited in Claim 51, wherein the temperature range of the semiconductor material during said plasma etching process is from about 40°C to about 130°C.

53. A method as recited in Claim 51, wherein said fluorinated chemical etchant comprises an etchant selected from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $C_2F_8$, $CH_2F_2$, $CHF_3$, $C_2HF_5$, and $CH_3F$.

54. A method as recited in Claim 50, wherein said plasma etching process is conducted at a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or for semiconductor material.

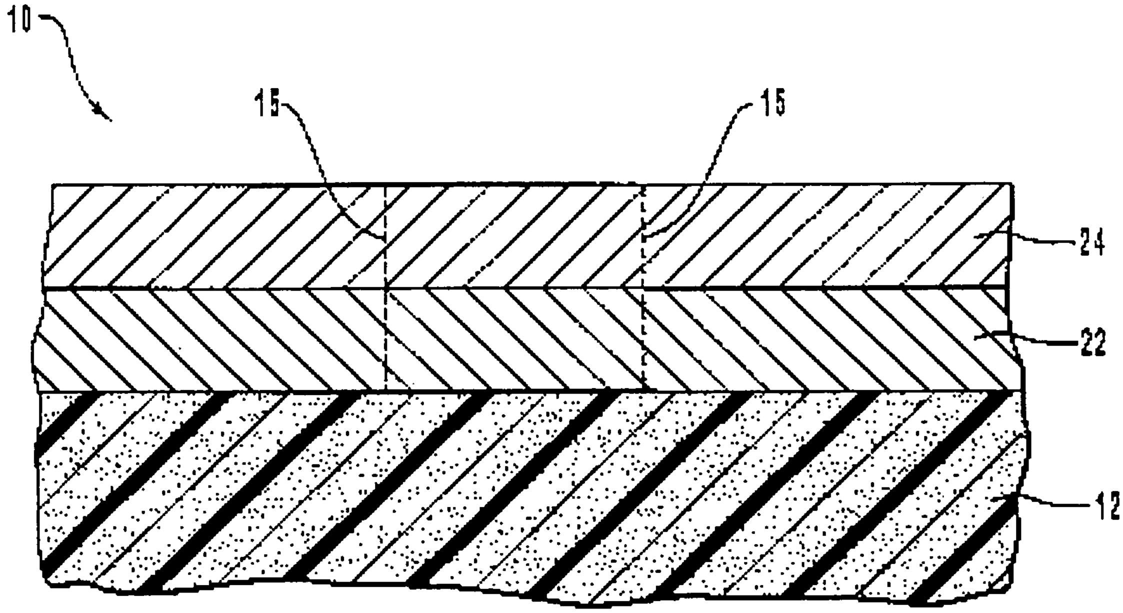


FIG. 1

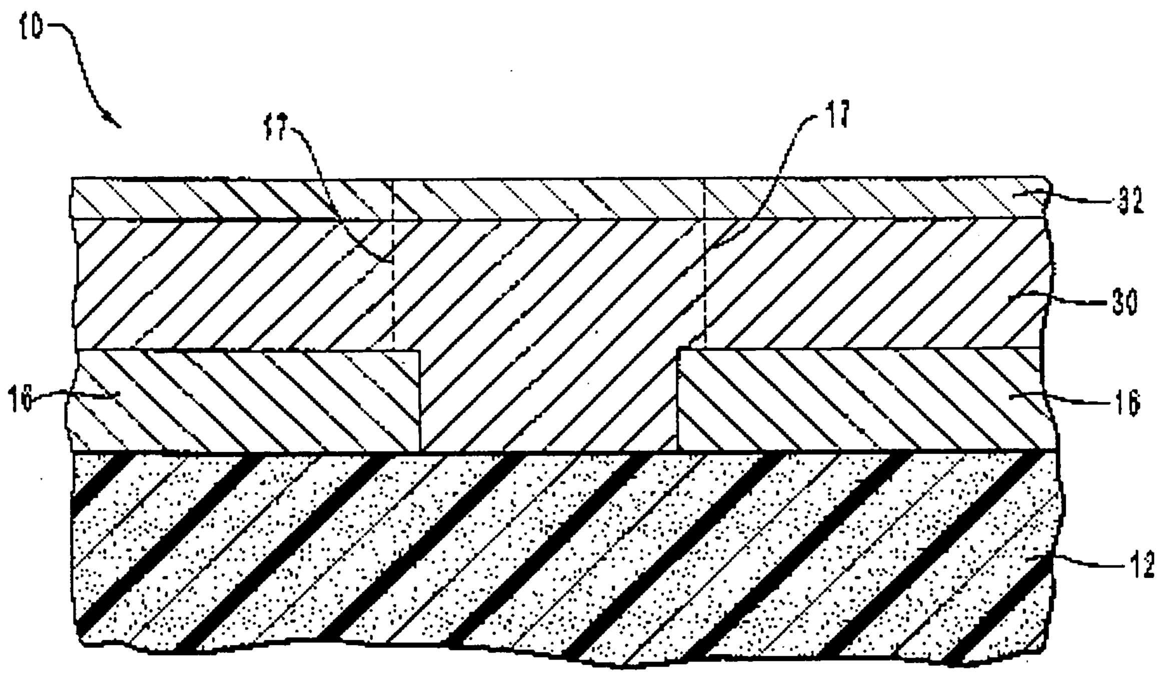


FIG. 2

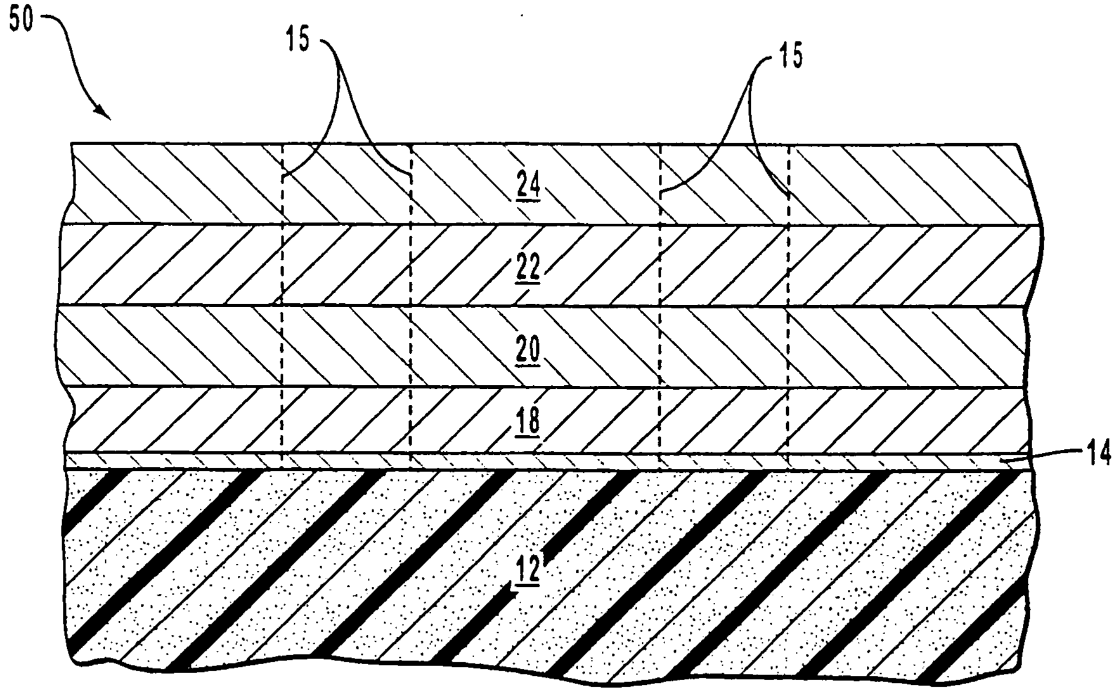

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FIG. 3

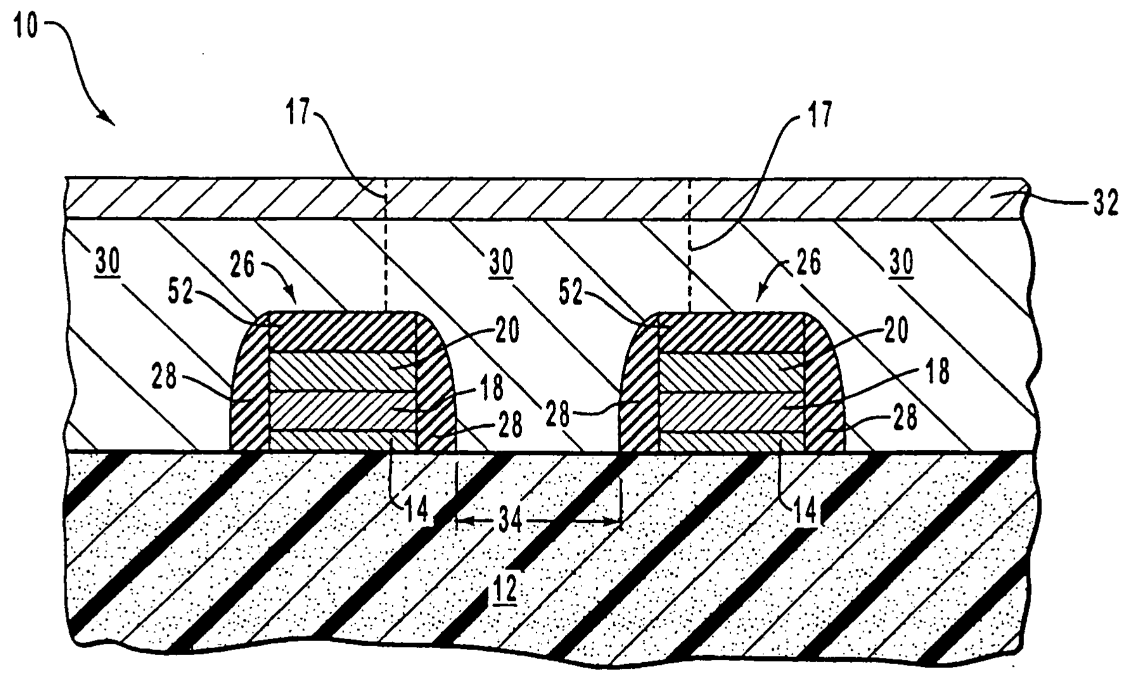

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FIG. 4